AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for generating a fully depleted body structure in a silicon-on-insulator device having a substrate, the method comprising:

providing an extractor contact coupled to the body structure in the silicon-on-insulator layer; and

providing an extractor voltage such that the extractor contact is reverse biased and minority carriers in the body structure are removed.

2. (Original) The method of claim 1 wherein the substrate is at ground potential.

3. (Original) The method of claim 1 wherein the extractor contact is coupled to a p-type silicon on the insulator.

4. (Original) The method of claim 1 wherein the extractor contact is coupled to an n-type silicon on the insulator.

5. (Original) The method of claim 1 wherein the silicon-on-insulator device has a drain region and the method further comprises applying a drain voltage to the drain region.

6. (Original) The method of claim 5 wherein the extractor voltage is greater than the drain voltage.

7. (Original) The method of claim 2 wherein the extractor voltage is less than the substrate potential.

8. (currently amended) A method for generating a fully depleted body structure in a PMOS silicon-on-insulator device having a substrate, a control gate, a drain region, and a source region, the method comprising:

applying an extractor voltage to an extractor contact coupled to the body structure in the silicon-on-insulator layer; and

applying a substrate voltage to the substrate such that the extractor voltage is greater than the substrate voltage.

9. (Original) The method of claim 8 wherein the substrate voltage is ground potential.

10. (Original) The method of claim 8 wherein the extractor contact is coupled to an n-type silicon on the substrate.

11. (Original) The method of claim 8 and further including applying a positive voltage to the control gate to erase a charge stored in the device.

12. (currently amended) A method for generating a fully depleted body structure in an NMOS silicon-on-insulator device having a substrate, a control gate, a drain region, and a source region, the method comprising:

applying an extractor voltage to an extractor contact coupled to the body structure in the silicon-on-insulator layer; and

applying a substrate voltage to the substrate such that the extractor voltage is less than the substrate voltage.

13. (Original) The method of claim 12 wherein the extractor contact is coupled to a p-type silicon on the substrate.

14. (Original) The method of claim 12 and further including applying a negative voltage to the control gate to erase a charge stored in the device.

15. (currently amended) A method for generating a fully depleted body region in an NROM flash memory device using a silicon-on-insulator structure, the device having a substrate, a control gate, a drain region, and a source region, the method comprising:

applying an extractor voltage to an extractor contact coupled to the body structure in the silicon-on-insulator layer; and

applying a substrate voltage to the substrate such that the extractor voltage is less than the substrate voltage.

16. (Original) The method of claim 15 wherein the extractor contact is comprised of a p-type silicon.

(17 – 22) Canceled.